Depletion-Merged FET Design in Bulk Silicon

TECHNICAL FIELD

[0001] The present invention relates generally to semiconductor devices manufactured in bulk silicon, and more particularly to such semiconductor devices having reduced reverse body effects and reduced parasitic junction capacitance similar to that available with PD-SOI (partially depleted silicon-on-insulator) semiconductors, but without the undesirable "floating body" effects of a PD-SOI transistor.

BACKGROUND

[0002] As will be appreciated by those skilled in the art, PD-SOI transistors are often favored over transistors manufactured in bulk silicon as providing several advantages including reduced junction capacitance and absence of the reverse body effects, etc. The PD-SOI transistor has a silicon body thickness that is thicker than the maximum depletion layer within the transistor such that a portion or region of the body of the PD-SOI transistor is undepleted. Since the undepleted body portions of the PD-SOI transistor is not tied or directly connected to any voltage, it is commonly referred to as being a "floating body" region. The "floating body" region causes undesirable effects in the PD-SOI device because of charges that accumulate in the floating body region, which is formed directly below the channel region. Although PD-SOI transistors are easily manufactured, the undesirable effects of the "floating body" region cause substantial variations in the circuit performance, which in turn presents very serious design challenges to the engineers.

[0003] Therefore, it would be advantageous if FET (field effect transistors) having reduced reverse body effects and reduced parasitic junction capacitance could be manufactured without the floating body effects of a PD-SOI transistor.

SUMMARY OF THE INVENTION

[0004] These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by preferred embodiments of the present invention, which discloses a field effect transistor formed on a bulk silicon substrate that has the advantages of reduced reverse body effects and reduced parasitic capacitance of a PD-SOI transistor, but not the disadvantages of the "floating body effects" also associated with PD-SOI transistors. The field effect transistor of this invention comprises a first source/drain region, a second source/drain region, a channel region separating the first and second source/drain regions and a depletion region defined under the channel region and between the first and second source/drain regions, where the depletion regions associated with the first and second source/drain regions have merged because of selected ion implantation of "graded" areas of the source/drain regions. A gate member is formed over the channel region in a normal manner. The field effect transistor shows improved characteristics where the depletion areas have only partially merged. However, the characteristics are most improved when the merged depletion region is a fully merged depletion region.

[0005] In a manner well known in the art, the field effect transistors found in the bulk silicon also typically include a pair of shallow oxide trenches for isolating said field effect transistor, (i.e., STI).

[0006] Although discussed above with respect to a single transistor, it will be appreciated that a multiplicity of field effect transistors will typically be formed in the bulk silicon substrate.

[0007] The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be

better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

[0009] FIG. 1 is a prior art illustration of an FET formed in bulk silicon;

[0010] FIG. 2A illustrates another prior art illustration of an FET formed in bulk silicon, and FIGs. 2B and 2C illustrate FET's formed in bulk silicon according to the present invention;

[0011] FIG. 3 is a graph comprising the "reverse body effects" of the FET structure of FIGs. 2A, 2B and 2C;

[0012] FIG. 4 is a graph illustrating the current leakage of an FET with fully merged depletion regions; and

[0013] FIG. 5 illustrates improvement in C_{jswg} parasitic capacitance of an FET employing a fully merged depletion region according to the teachings of the present invention.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0014] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0015] Referring now to FIG. 1, there is illustrated a prior art bulk silicon device. As shown in FIG. 1, there is included a bulk silicon substrate 10. The term "bulk silicon" is used to include a semiconductor device formed in a layer or wafer of silicon having a substantial thickness as indicated by double-headed arrow 12 and to distinguish from a SOI (silicon-on-insulator) structure, which forms semiconductor devices in a thin layer of silicon.

[0016] The formation of an FET semiconductor device formed in the bulk silicon will now be described. A first graded source/drain region, such as source region 14 and a second graded source/drain region, such as drain region 16 is formed in the bulk silicon 10 by ion implantation. Extending between the source region 14 and drain region 16 is a channel region 18. As mentioned, the source regions and drain regions 14 and 16, respectively, are "graded" implant regions as indicated by the two areas 14a and 14b and 16a and 16b associated with a pair of source/drain regions as formed by two different ion implantations. A gate oxide 20 is formed over the channel region 18 and a poly silicon gate 22 is formed on top of the gate oxide to complete the field effect transistor. A pair of STI (shallow trench isolation) regions 24a and 24b is also typically included to separate the field effect transistor from other circuits or field effect transistors formed in the bulk silicon 10. Other techniques for isolating devices, such as the

formation of field oxide areas, could of course be used. Of particular interest according to the present invention, is the dotted line area 26, which includes an electron depletion region 28 between the source 14 and drain 16 regions and for a short distance below the channel region 18.

[0017] Referring now to FIGs. 2A, 2B and 2C, there is illustrated variations in the area of interest 26 according to the present invention. Those portions of FIGs. 2A, 2B and 2C that are equivalent to the elements of FIG. 1 will carry the same reference number. Therefore, FIG. 2A illustrates that the graded source regions 14a and 14b are very close to the drain regions 16a and 16b but do not touch, and therefore, the depletion area has not merged. FIG. 2B on the other hand, shows a partially merging of the depletion area and FIG. 2C shows the source and drain areas 14 and 16 overlapping, which results in fully merged depletion regions. Thus, it is seen that the merged depletion area is a result of the overlapping of the graded source/drain regions, which in turn is a result of optimizing the location and density of the ion implantation step used to form the graded source and drain regions 14 and 16. It has been determined that an ion implantation density of between about E^{12}/cm^2 to about $5E^{13}/cm^2$ is particularly suitable for use with the invention. As was discussed above, advantages of the PD-SOI transistor structure are the reduced parasitic capacitance and the reduced reverse body effects.

[0018] Referring now to FIG. 3, there is illustrated the significantly reduced reverse body effects obtained by fully merging the depletion regions according to the teachings of the present invention. As shown in the structure of FIG. 2A, the depletion regions are not merged and the reverse body effects for the structure of FIG. 2A are illustrated by curve 30a. As can be seen, the $V_{t(sat)}$ is about 60 milivolts at a V_{bs} (V_{bs} = voltage bias between the substrate and the source) of 1.2 volts. Curve 30B of FIG. 3B illustrates the reverse body effects for the partially merged depletion region structure of FIG. 2B. As shown at a V_{bs} of –1.2 volts, the $V_{t(sat)}$ has improved to

about 44 milivolts, but is still high. However, curve 30c, which illustrates the reverse body effects of the fully merged depletion region structure of FIG. 3C has been significantly reduced to less than 20 milivolts.

[0019] In addition, it has been discovered that the merging of the depletion region results in a reduction of the DIBL (drain induced barrier lowering). The sub-threshold swing at high V_{ds} (V_{ds} = high-drain-to source bias) is not significantly degraded (such that the IDBL resulting from the depletion merging may be less than that resulting from short channel effects. Significantly it is seen by referring to FIG. 4 that merging of the depletion regions results in very small current leakage at the merged region. That is, there is no increase in the risk of source/drain punch-through. More specifically, the curve of FIG. 4 illustrates the current density as a function of the distance from the gate oxide. Although there is a slight increase in the amount of leakage in the merged region at a location of about 0.9 micrometers from the gate oxide as indicated by reference number 32, the amount of leakage is still negligible or about $1E^{-7}$ amps/centimeters^2 as shown.

[0020] Referring again to FIG. 1, the parasitic capacitance C_{jb}, C_{jsw}, and C_{jswg} indicated by reference numbers 34, 36 and 38, respectively, are illustrated. Parasitic capacitance and more specifically the high sidewall gate capacitance C_{jswg} 38 degrade the AC performance of the transistor. However, as shown in the graph of FIG. 5, merging the depletion region of the transistor also results in a significant reduction in the C_{jswg} capacitance. As shown, the depletion region according to this invention results in about a 45% reduction. The C_{jswg} capacitance versus the V_{bs} for a prior art transistor is indicated by curve 40 and the depletion-merged transistor of the present invention is illustrated by curve 42.

[0021] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

[0022] Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.